

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

INTRODUCTION

The KS0070B is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology.

FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 80 segment signal output.
- Easy Interface with a 4-bit or 8-bit MPU
- Display character pattern:
 - 5 x 7 dots format : 192 kinds, 5x10 dots format : 32 kinds
- The special character pattern can be programmable by character generator RAM directly.
- A customer character pattern can be programmable by mask option. (KS0070B-00: Standard type)

KS0070B-00

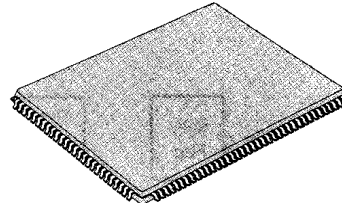
English, Japanese Numeral

- Automatic power on reset function.
- It can drive a maximum 80 characters by using the KS0065B or KS0063 externally.
- It is possible to read both Character Generator and Display Data RAM from MPU.

FEATURES

- Internal Memory
 - Character Generator ROM : 8320bits
 - Character Generator RAM : 512 bits
 - Display Data RAM : 80x8bits for 80 digits.
- Power Supply Voltage ; +5V \pm 10%, +3V \pm 10%
- Supply voltage for display: 0 ~ -5V(V5)
- CMOS process
- 1/8 duty, 1/11 duty or 1/16 duty : selectable
(1/8 duty ; 5x7 dots format 1 line, 1/11 duty ; 5x10 dots format 1 line,
1/16 duty: 5x7 dots format 2 line)
- 128 QFP, bare chip available or bumped chip.

128 QFP



SAMSUNG

ELECTRONICS

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

BLOCK DIAGRAM

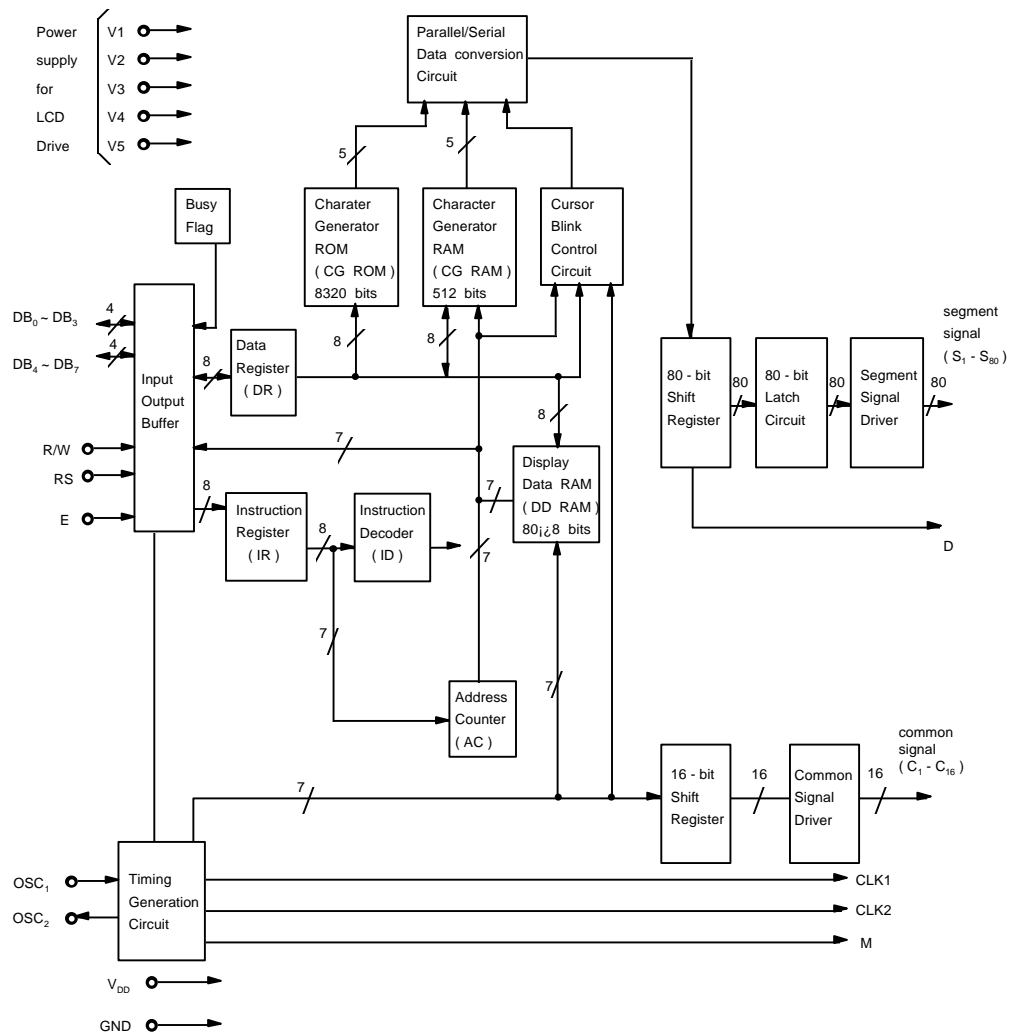


Fig. 1. KS0070B functional block diagram.

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

PIN CONFIGURATION

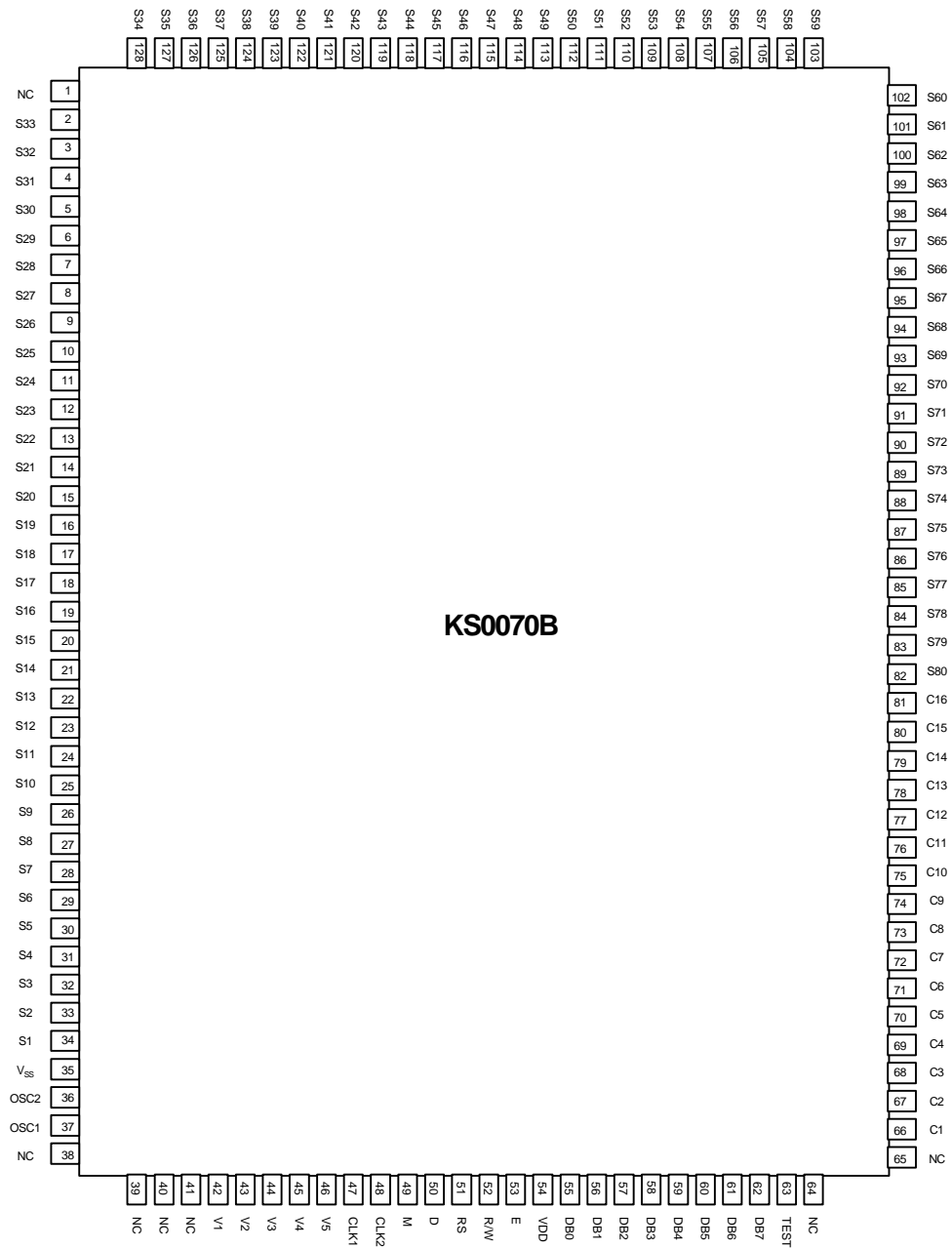


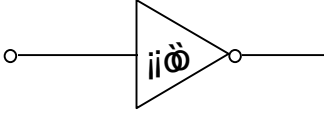
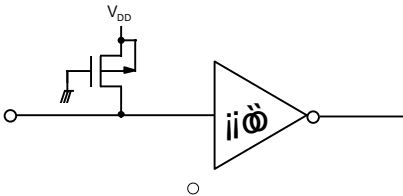
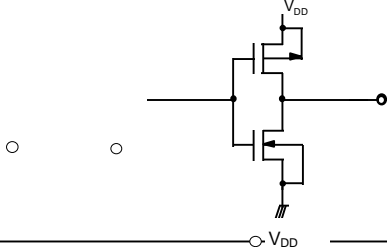
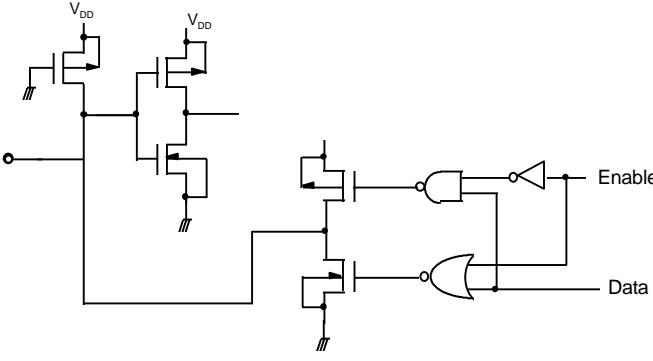
Fig. 2. 128 QFP Top View

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

PIN DESCRIPTION

PAD(NO)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE				
V _{DD} (54)	Power	Operating Voltage	for logical circuit(+5V±10%,+3V±10%)	Power supply				
V _{SS} (GND)(35)			0V(GND)					
V ₁ -V ₅ (42-46)		Negative Supply Voltage	Bias voltage level for LCD driving					
S ₁ -S ₂₃ , S ₃₄ -S ₈₀ (34-2, 128-82)	Output	Segment output	Segment signal output for LCD driving	LCD				
C ₁ -C ₁₆ (66-81)	Output	Common output	Common signal output for LCD driving	LCD				
OSC, OSC2 (37, 36)	Input(OSC1) Output(OSC2)	Oscillator	Both pin connected to Rf resistor or Ceramic resonator for internal oscillator circuit. In case of external frequency use only, the frequency is input to OSC1 terminal.	Resistor or Ceramic Resonator				
CLK1 (47)	Output	Data latch clock	Clock output terminal for the serially transferred data to be latched to the driver.	KS0065B or KS0063				
CLK2 (48)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.					
M(49)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC					
D(50)		Display data interface	Character pattern data, which is corresponding to each common signal, is supplied to driver serially. <table border="1" style="margin-left: 20px;"> <tr> <td>High</td> <td>Selection</td> </tr> <tr> <td>Low</td> <td>Non selection</td> </tr> </table>		High	Selection	Low	Non selection
High	Selection							
Low	Non selection							
E(53)	Input	Enable	Start enable signal to read or write the data	MPU				
R/W(52)		Read/Write	R/W signal input is used to select the read/write mode <table border="1" style="margin-left: 20px;"> <tr> <td>High</td> <td>Read mode</td> </tr> <tr> <td>Low</td> <td>Write mode</td> </tr> </table>		High	Read mode	Low	Write mode
High	Read mode							
Low	Write mode							
RS(51)	Input	Register select	Register selection input <table border="1" style="margin-left: 20px;"> <tr> <td>High</td> <td>Data register (for read and write)</td> </tr> <tr> <td>Low</td> <td>Instruction register(for write), Busy flag, address counter (for read)</td> </tr> </table>	High	Data register (for read and write)	Low	Instruction register(for write), Busy flag, address counter (for read)	MPU
High	Data register (for read and write)							
Low	Instruction register(for write), Busy flag, address counter (for read)							
DB ₀ -DB ₇ (55-62)	Input/Output	Data interface	Used for data transfer between the MPU and KS0070B /70BM These terminals are for data bus with bidirectional three-state. Initial 4 bit(DB ₀ -DB ₃) are not used during 4-bit operation(DB ₇ can be used as a busy flag)	MPU				
TEST(63)	Test pin	Input	This pin must be fixed to V _{DD} or open					

Internal logic of input/output terminal

Input/Output	Logic diagram		Applicable pin
Input	No Pull up		E
	with pull up		RS, R/W
Output			CLK1, CLK2 M, D
Input Output			DB ₀ - DB ₇

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MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 ~ + 7.0	V
Driver Supply Voltage	V_{LCD}	$V_{DD} - 15.0 \sim V_{DD} + 0.3$	V
Input Voltage	V_{IN}	- 0.3 ~ $V_{DD} + 0.3$	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	- 30 ~ + 85	°C
Storage Temperature	T_{STG}	- 55 ~ + 125	°C

* Voltage greater than above may damage the circuit ($V_{D0} \geq V_{D1} \geq V_{D2} \geq V_{D3} \geq V_{D4} \geq V_{D5}$)

ELECTRICAL CHARACTERISTICS

DC Characteristics ($V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic	Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin		
Operating Voltage	V_{DD}	-	4.5	-	5.5	V			
Operating Current(*1)	I_{DD1}	Ceramic resonator fosc=250KHz	-	0.7	1.0	mA			
	I_{DD2}	Resistor oscillation external clock operation fosc=270KHz	-	0.4	0.6				
Input Voltage 1	High	V_{IH1}	-	2.2	-	V_{DD}	E, OB ₀ -DB ₇ , R/W, RS		
	Low	V_{IL1}	-	-0.3	-			0.6	
Input Voltage 2	High	V_{IH2}	-	$V_{DD}-1.0$	-	V_{DD}	OSC1		
	Low	V_{IL2}	-	-0.2	-			1.0	
Output Voltage 1	High	V_{OH1}	$I_{OH} = -0.205mA$	2.4	-	V	DB ₀ -DB ₇		
	Low	V_{OL1}	$I_{OL} = 1.2mA$	-	-			0.4	
Output Voltage 2	High	V_{OH2}	$I_O = -40\mu A$	$0.9V_{DD}$	-	-	CLK1, CLK2, M, D		
	Low	V_{OL2}	$I_O = 40\mu A$	-	-			$0.1V_{DD}$	
Voltage Drop (*2)	COM	V_{dCOM}	$I_O = \pm 0.1mA$	-	-	1	C1-C16 S1-S80		
	SEG	V_{dSEG}		-	-			1	
Input Leakage Current	I_{LKG}	$V_{IN} = 0$ or V_{DD}	-1	-	1	μA	E		
Input Low Current	I_{IL}	$V_{DD} = 5V$ (test pull up R)	-50	-125	-250		RS, R/W, DB ₀ -DB ₇		
External Clock	Frequency(*3)	f_{EC}	-	15	250	350	KHz	OSC1	
	Duty	duty	-	45	50	55			%
	Rise Time	t_R	-	-	-	0.2			μS
	Fall Time	t_F	-	-	-	0.2			μS
Internal Clock Frequency(*3)	f_{OSC1}	Rf=91K±2%	190	270	350	KHz	OSC1, OSC2		
Ceramic Resonator Oscillation Frequency(*3)	f_{OSC2}	-	245	250	255				
LCD Driving Voltage(*4)	V_{LCD1}	$V_{DD} - V_5$	1/5 bias	4.6	-	10	V		
	V_{LCD2}		1/4 bias	3.0	-	10			

Note (*1) : Applies to the current value flow in terminal V_{DD} when power is input as follows; $V_{DD} = 5V$, $GND = 0V$, $V_1 = 3.4V$, $V_2 = 1.8V$, $V_3 = 0.2V$, $V_4 = -1.4V$ and $V_5 = -3V$.

(*2) : Applied to the voltage drop occurring from terminals V_{DD} , V_1 , V_4 and V_5 to each common terminal (C1-C16) when 0.1mA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occurring from terminals V_{DD} , V_2 , V_3 and V_5 to each SEG terminal (S1-S80). When the output level is at V_{DD} , V_1 or V_2 level, 0.1mA is flown out, while 0.1mA flow in when the output level is at V_3 , V_4 , or V_5 level. This occurs when 5V or -5V is input to V_{DD} , V_1 and V_3 or to V_2 , V_4 , and V_5 respectively.

(*3) and (*4) : Refer to oscillator circuit and input the voltage listed in the table below to $V_1 - V_5$

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ELECTRIC CHARACTERISTICS (continued) DC Characteristics ($V_{DD} = +3V \pm 10\%$, $V_{SS} = 0V$, $T_a = -30 \sim +85^\circ C$)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	-	2.7	3.0	3.3	V	-
Operating Current(*1)		I_{DD1}	Ceramic resonator $f_{osc} = 250KHz$	-	0.3	0.5	mA	-
		I_{DD2}	Resistor oscillation external clock operation $f_{osc} = 270KHz$	-	0.17	0.3		
Input Voltage 1	High	V_{IH1}	-	1.9	-	V_{DD}	V	E, OB ₀ -DB ₇ , R/W, RS
	Low	V_{IL1}	-	-0.3	-	0.4		
Input Voltage 2	High	V_{IH2}	-	$0.7V_{DD}$	-	V_{DD}		OSC1
	Low	V_{IL2}	-	-	-	$0.2V_{DD}$		
Output Voltage 1	High	V_{OH1}	$I_{OH} = -0.1mA$	2.0	-	-		DB ₀ -DB ₇
	Low	V_{OL1}	$I_{OL} = +0.1mA$	-	-	0.4		
Output Voltage 2	High	V_{OH2}	$I_O = -40\mu A$	$0.8V_{DD}$	-	-		CLK1, CLK2, M, D
	Low	V_{OL2}	$I_O = +40\mu A$	-	-	$0.2V_{DD}$		
Voltage Drop (*2)	COM	V_{dCOM}	$I_O = \pm 0.05mA$	-	-	1	C1-C16	
	SEG	V_{dSEG}		-	-	1.5	S1-S80	
Input Leakage Current		I_{LKG}	$V_{IN} = 0$ or V_{DD}	-1	-	1	μA	E
Input Low Current		I_{IL}	$V_{DD} = 3V$ (test pull up R)	-10	-50	-120		RS, R/W, DB ₀ -DB ₇
External Clock	Frequency(*3)	f_{EC}	-	125	250	350	KHz	OSC1
	Duty	duty		45	50	55	%	
	Rise time	t_R		-	-	0.2	μs	
	Fall time	t_F		-	-	0.2	μs	
Internal Clock Frequency(*3)		f_{OSC}	$R_f = 75K\Omega \pm 2\%$	190	270	350	KHz	OSC1, OSC2
LCD driving voltage(*4)		V_{LCD1}	1/5 bias	3.0	-	10.0	V	V1 ~ V5
		V_{LCD2}	1/4 bias	3.0	-	10.0		

Note (*1) : The supply current value from V_{DD} when the power condition is as follows

$V_{DD} = 5V$, $V_{SS} = 0V$, $V_5 = -2V$ (when $V_{DD} = 5V$)

$V_{DD} = 3V$, $V_{SS} = 0V$, $V_5 = -2V$ (when $V_{DD} = 3V$)

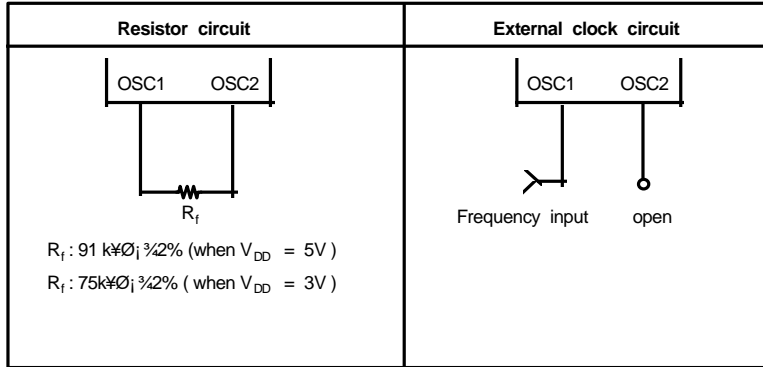
(*2) : The voltage drop from LCD bias terminals V_{DD} , V1, V4 and V5 to each common terminal (C1 ~ C16).

and also the voltage drop from LCD bias terminals V_{DD} , V2, V3 and V5 to each segment terminal (S1 ~ S80)

(*3) and (*4) : Refer to oscillator circuit and input the voltage listed in the table below to $V_1 - V_5$

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(*3) Oscillator circuit



(*4) Input the voltage listed in the table below to $V_1 - V_5$

	Duty	1/8, 1/11	1/16
	Bias	1/4	1/5
V_1		$V_{DD} - \frac{V_{LCD}}{4}$	$V_{DD} - \frac{V_{LCD}}{5}$
V_2		$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{2V_{LCD}}{5}$
V_3		$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{3V_{LCD}}{5}$
V_4		$V_{DD} - \frac{3V_{LCD}}{4}$	$V_{DD} - \frac{4V_{LCD}}{5}$
V_5		$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

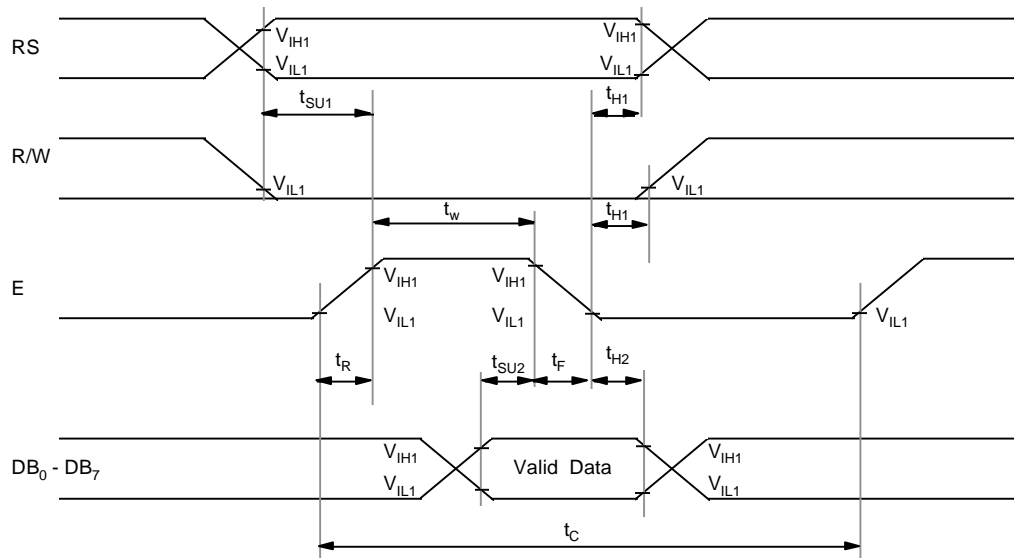
* V_{LCD} is the LCD driving voltage , refer to the initial set of the instruction code.

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

AC Characteristics ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -30^\circ C \sim +85^\circ C$)

(1) Write mode (Writing data from Microm to KS0070B)

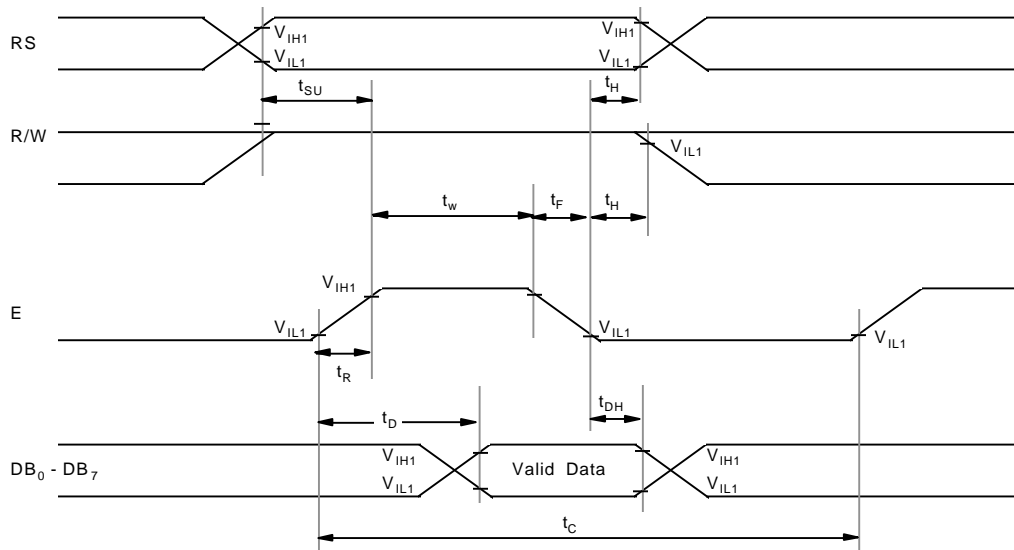
Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	500	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_w	220	-	-	ns	E
R/W And RS Set-Up Time	t_{SU1}	40	-	-	ns	R/W, RS
R/W And RS Hold Time	t_{H1}	10	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	60	-	-	ns	DB ₀ ~ DB ₇
Data Hold Time	t_{H2}	10	-	-	ns	DB ₀ ~ DB ₇



(2) Read mode (Reading data from KS0070B to Microm)

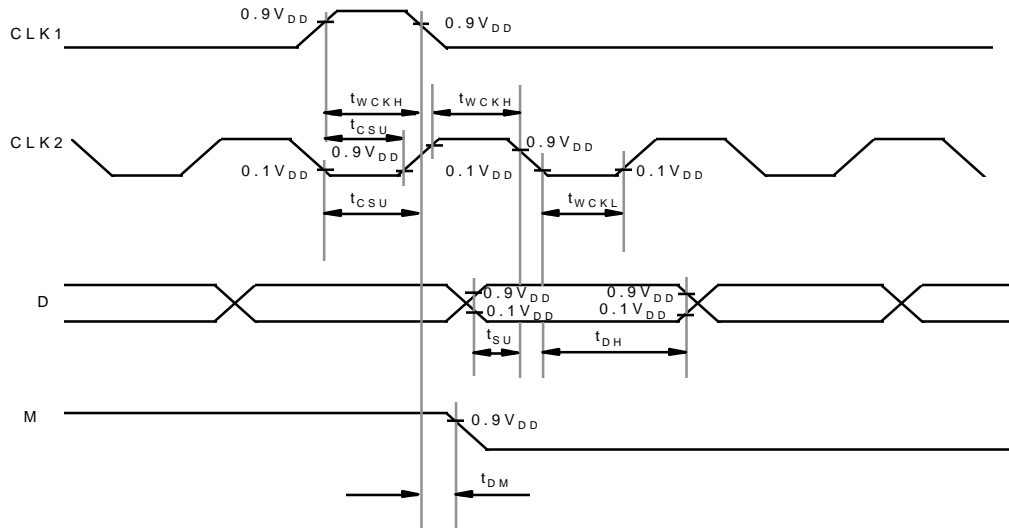
Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	500	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_w	220	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	40	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	10	-	-	ns	R/W, RS
Data Output Delay Time	t_D	-	-	120	ns	DB ₀ ~ DB ₇
Data Hold Time	t_{DH}	20	-	-	ns	DB ₀ ~ DB ₇

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(3) Interface mode with KS0065B, KS0063

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock Pulse Width High	t_{WCKH}	800	-	-	ns	CLK
Clock Pulse Width Low	t_{WCKL}	800	-	-	ns	CLK
Data Set-Up Time	t_{SU}	300	-	-	ns	D
Data Hold Time	t_{DH}	300	-	-	ns	D
Clock Set-Up Time	t_{CSU}	500	-	-	ns	CLK
M Delay Time	t_{DM}	-1000	-	1000	ns	M



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AC Characteristics ($V_{DD} = 3V \pm 10\%$, $V_{SS} = 0V$, $T_a = -30^\circ C \sim +85^\circ C$)

(1) Write mode (Writing data from Micom to KS0070B)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	1400	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_w	400	-	-	ns	E
R/W And RS Set-Up Time	t_{SU1}	60	-	-	ns	R/W, RS
R/W And RS Hold Time	t_{H1}	20	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	140	-	-	ns	DB ₀ ~ DB ₇
Data Hold Time	t_{H2}	10	-	-	ns	DB ₀ ~ DB ₇

(2) Read mode (Reading data from KS0070B to Micom)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	1400	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_w	400	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	60	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	20	-	-	ns	R/W, RS
Data Output Delay Time	t_D	-	-	360	ns	DB ₀ ~ DB ₇
Data Hold Time	t_{DH}	5	-	-	ns	DB ₀ ~ DB ₇

(3) Interface mode with KS0065B, KS0063

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock Pulse Width High	t_{WCKH}	800	-	-	ns	CLK
Clock Pulse Width Low	t_{WCKL}	800	-	-	ns	CLK
Data Set-Up Time	t_{SU}	300	-	-	ns	D
Data Hold Time	t_{DH}	300	-	-	ns	D
Clock Set-Up Time	t_{CSU}	500	-	-	ns	CLK
M Delay Time	t_{DM}	-1000	-	1000	ns	M

CONTROL and DISPLAY COMMAND

Command	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	Execution time (fosc=250KHz)	Remark																		
DISPLAY CLEAR	L	L	L	L	L	L	L	L	L	H	1.64ms																			
RETURN HOME	L	L	L	L	L	L	L	L	L	H	X	1.64ms	cursor move to first digit																	
ENTRY MODE SET	L	L	L	L	L	L	L	L	H	I/D	SH	42μs	<ul style="list-style-type: none"> I/D: set cursor move direction <table border="1"> <tr> <td>I/D</td> <td>H</td> <td>Increase</td> </tr> <tr> <td>I/D</td> <td>L</td> <td>Decrease</td> </tr> </table> SH: Specifies shift of display <table border="1"> <tr> <td>SH</td> <td>H</td> <td>display is shifted</td> </tr> <tr> <td>SH</td> <td>L</td> <td>display is not shifted</td> </tr> </table> 	I/D	H	Increase	I/D	L	Decrease	SH	H	display is shifted	SH	L	display is not shifted					
I/D	H	Increase																												
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SH	H	display is shifted																												
SH	L	display is not shifted																												
DISPLAY ON/OFF	L	L	L	L	L	L	H	D	C	B	42μs	<ul style="list-style-type: none"> Display <table border="1"> <tr> <td>D</td> <td>H</td> <td>Display on</td> </tr> <tr> <td>D</td> <td>L</td> <td>Display off</td> </tr> </table> Cursor <table border="1"> <tr> <td>C</td> <td>H</td> <td>Cursor on</td> </tr> <tr> <td>C</td> <td>L</td> <td>Cursor off</td> </tr> </table> Blinking <table border="1"> <tr> <td>B</td> <td>H</td> <td>Blinking on</td> </tr> <tr> <td>B</td> <td>L</td> <td>Blinking off</td> </tr> </table> 	D	H	Display on	D	L	Display off	C	H	Cursor on	C	L	Cursor off	B	H	Blinking on	B	L	Blinking off
D	H	Display on																												
D	L	Display off																												
C	H	Cursor on																												
C	L	Cursor off																												
B	H	Blinking on																												
B	L	Blinking off																												
SHIFT	L	L	L	L	L	H	S/C	R/L	X	X	42μs	<table border="1"> <tr> <td rowspan="2">SC</td> <td>H</td> <td>Display shift</td> </tr> <tr> <td>L</td> <td>Cursor move</td> </tr> <tr> <td rowspan="2">R/L</td> <td>H</td> <td>Right shift</td> </tr> <tr> <td>L</td> <td>Left shift</td> </tr> </table>	SC	H	Display shift	L	Cursor move	R/L	H	Right shift	L	Left shift								
SC	H	Display shift																												
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	L	Left shift																												
SET FUNCTION	L	L	L	L	H	DL	N	F	X	X	42μs	<table border="1"> <tr> <td rowspan="2">DL</td> <td>H</td> <td>8 bits interface</td> </tr> <tr> <td>L</td> <td>4 bits interface</td> </tr> <tr> <td rowspan="2">N</td> <td>H</td> <td>2 line display</td> </tr> <tr> <td>L</td> <td>1 line display</td> </tr> <tr> <td rowspan="2">F</td> <td>H</td> <td>5_i 10 dots</td> </tr> <tr> <td>L</td> <td>5_i 7 dots</td> </tr> </table>	DL	H	8 bits interface	L	4 bits interface	N	H	2 line display	L	1 line display	F	H	5 _i 10 dots	L	5 _i 7 dots			
DL	H	8 bits interface																												
	L	4 bits interface																												
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	L	1 line display																												
F	H	5 _i 10 dots																												
	L	5 _i 7 dots																												

Table 1.

KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

CONTROL and DISPLAY COMMAND (continued)

Command	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	Excution time (fosc=250KHz)	Remark						
SET CG RAM ADDRESS	L	L	L	H	CG RAM address (corresponds to cursor address)						42μs	CG RAM Data is sent and received after this setting						
SET DD RAM ADDRESS	L	L	H	DD RAM address								42μs	DD RAM Data is sent and received after this setting					
READ BUSY FLAG & ADDRESS	L	H	BF	Address Counter used for Both DD & CG RAM address							0μs	<table border="1" style="display: inline-table;"> <tr> <td>BF</td> <td>H</td> <td>Busy</td> </tr> <tr> <td></td> <td>L</td> <td>Ready</td> </tr> </table> <p>- Reads BF indication internal operating is being performed. - reads address counter contents</p>	BF	H	Busy		L	Ready
BF	H	Busy																
	L	Ready																
WRITE DATA	H	L	Read Data								46	Write data into DD or CGRAM						
READ DATA	H	H	Write Data								46μs	Read data from DD or CGRAM						

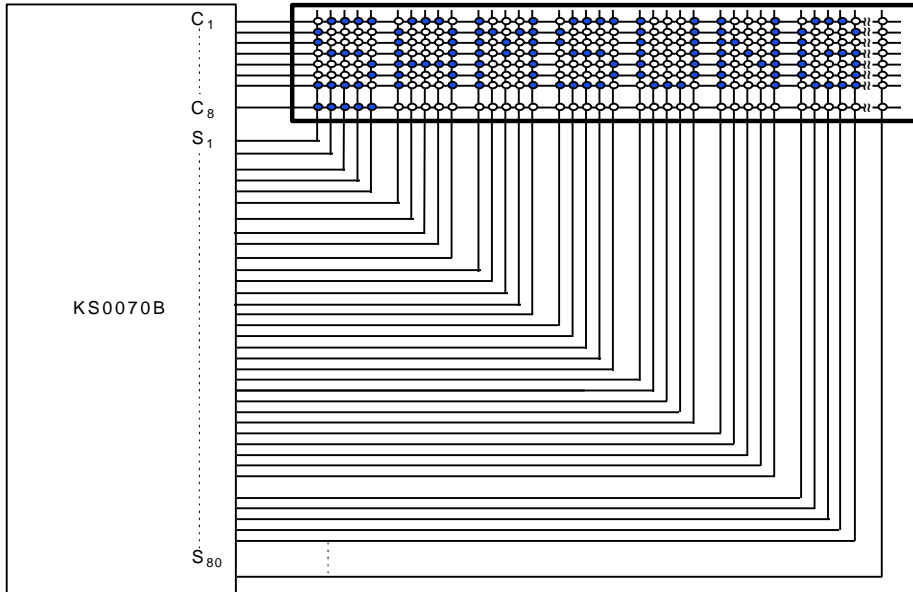
X: Don't care
Table 1



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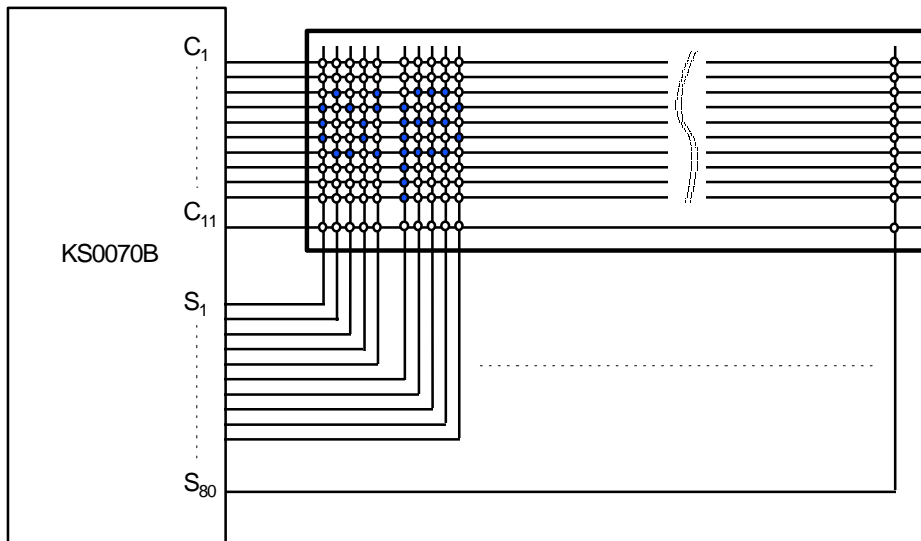
APPLICATION INFORMATION ACCORDING TO LCD PANEL

1) LCD Panel: 16 character x 1 line character format; 5x7 dots + 1 cursor line (1/4 bias, 1/8 duty)



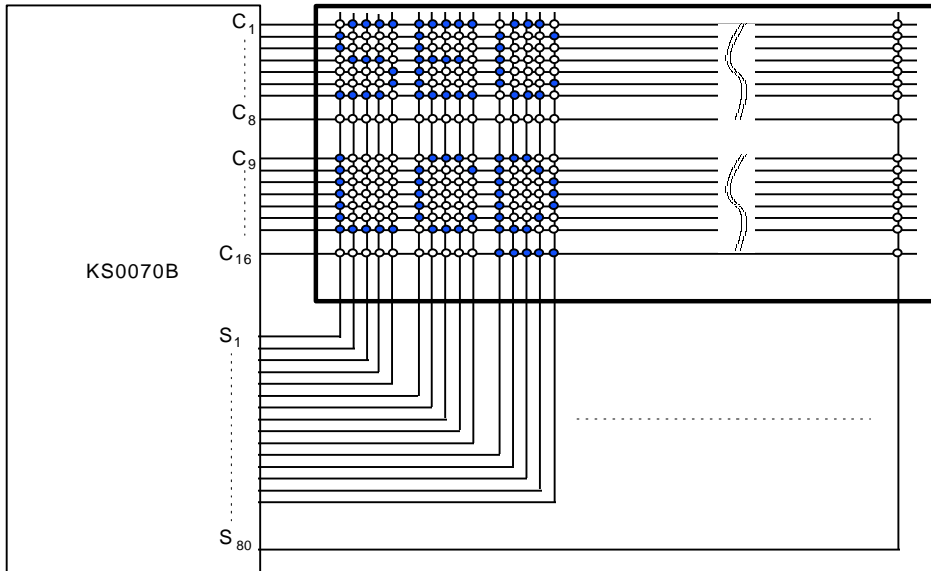
dots + 1 cursor line (1/4 bias, 1/11 duty)

2) LCD Panel: 16 character x 1 line character format; 5_i x 10

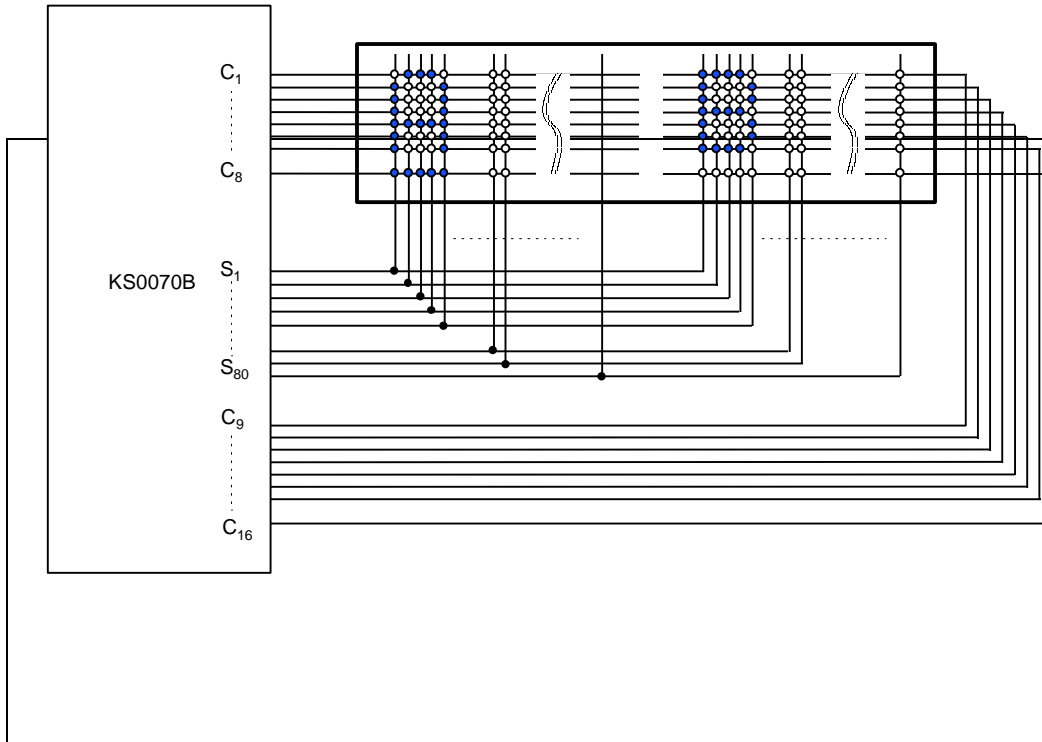


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3) LCD Panel: 16 characterx 2 line character format; 57dots + 1 cursor line (1/5 bias, 1/16 duty)

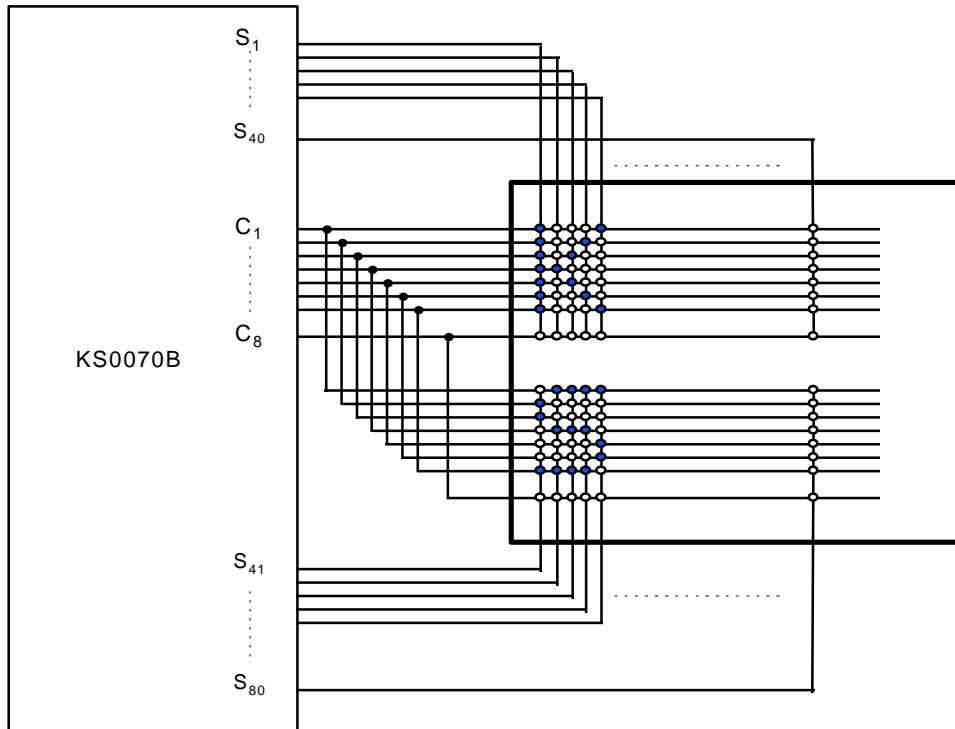


4) LCD Panel: 32 characterx1 line Character format; 5x7 dots + 1 cursor line (1/5 bias, 1/16 duty)

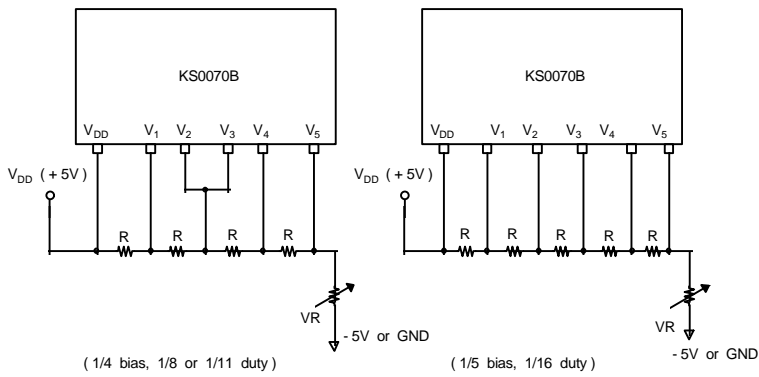


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5) LCD Panel: 8 characterx2 line character; 5x7 dot + 1 cursor line (1/4 bias, 1/8 duty)

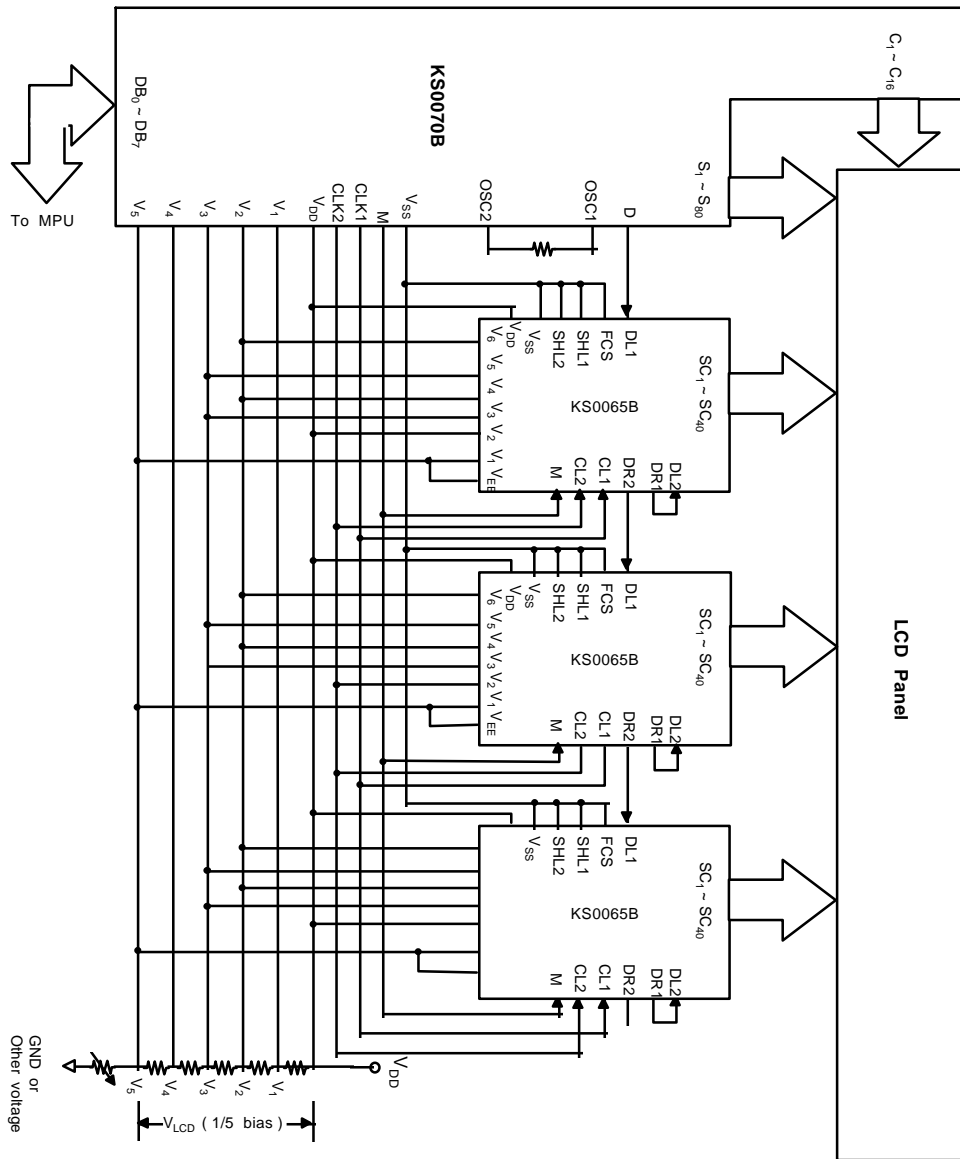


BIAS VOLTAGE DIVIDE CIRCUIT



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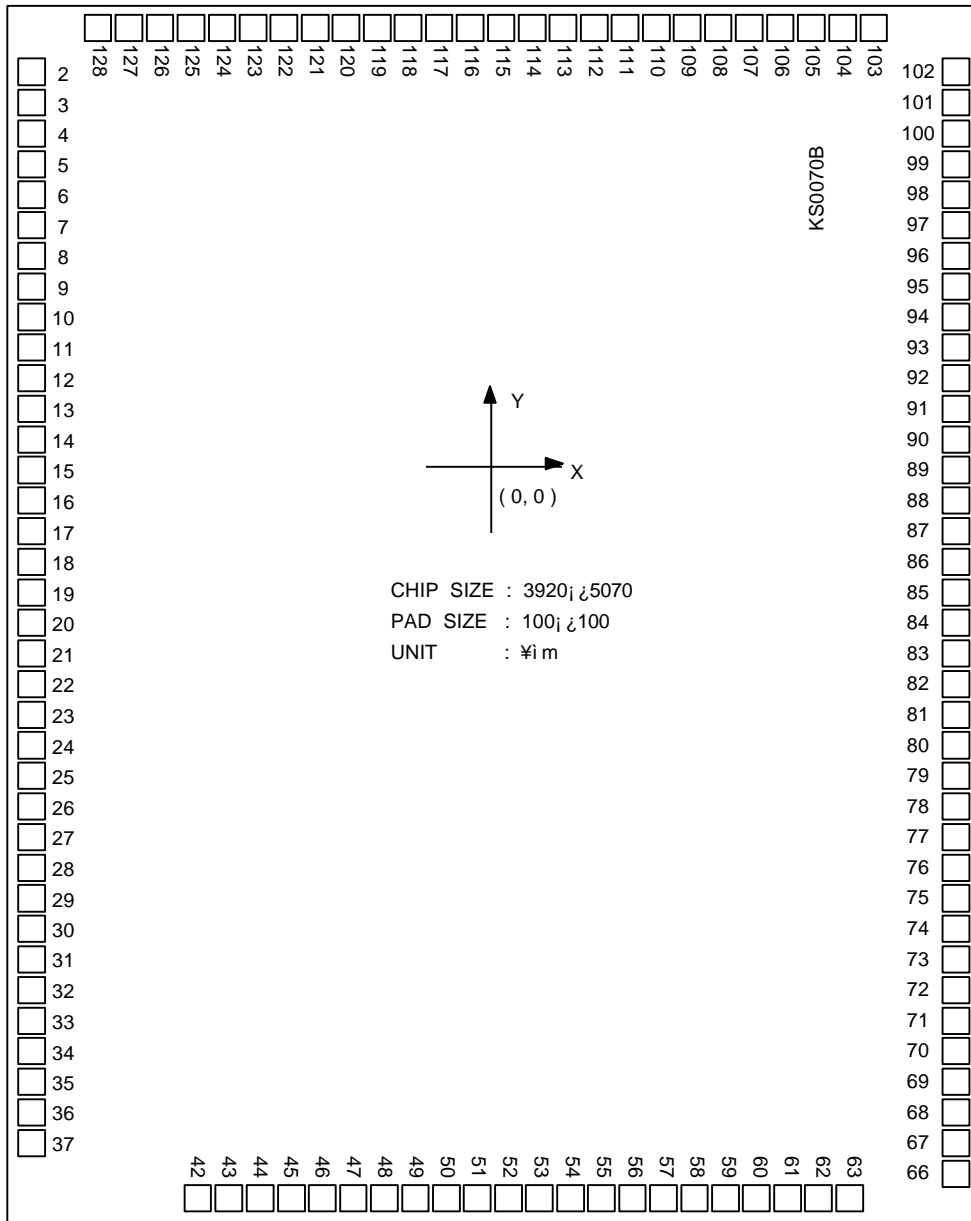
APPLICATION CIRCUIT



When KS0065B is externally connected to the KS0070B, you can increase the number of display digits up to 80 characters.

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PAD DIAGRAM



* "KS0070B" Marking : easy to find the PAD No. 98



KS0070B 16COM/80SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1		NC		37	OSC1	-1794	-2231	73	C8	1794	-1456
2	S33	-1794	2169	38		NC		74	C9	1794	-1331
3	S32	-1794	2044	39		NC		75	C10	1794	-1206
4	S31	-1794	1919	40		NC		76	C11	1794	-1081
5	S30	-1794	1794	41		NC		77	C12	1794	-956
6	S29	-1794	1669	42	V1	-1155	-2369	78	C13	1794	-831
7	S28	-1794	1544	43	V2	-1030	-2369	79	C14	1794	-706
8	S27	-1794	1419	44	V3	-905	-2369	80	C15	1794	-581
9	S26	-1794	1294	45	V4	-780	-2369	81	C16	1794	-456
10	S25	-1794	1169	46	V5	-655	-2369	82	S80	1794	-331
11	S24	-1794	1044	47	CLK1	-530	-2369	83	S79	1794	-206
12	S23	-1794	919	48	CLK2	-405	-2369	84	S78	1794	-81
13	S22	-1794	794	49	M	-280	-2369	85	S77	1794	44
14	S21	-1794	669	50	D	-155	-2369	86	S76	1794	169
15	S20	-1794	544	51	RS	-30	-2369	87	S75	1794	294
16	S19	-1794	419	52	RAW	96	-2369	88	S74	1794	419
17	S18	-1794	294	53	F	220	-2369	89	S73	1794	544
18	S17	-1794	169	54	VDD	345	-2369	90	S72	1794	669
19	S16	-1794	44	55	DB0	470	-2369	91	S71	1794	794
20	S15	-1794	-81	56	DB1	595	-2369	92	S70	1794	919
21	S14	-1794	-206	57	DB2	720	-2369	93	S69	1794	1044
22	S13	-1794	-331	58	DB3	845	-2369	94	S68	1794	1169
23	S12	-1794	-456	59	DB4	970	-2369	95	S67	1794	1294
24	S11	-1794	-581	60	DB5	1095	-2369	96	S66	1794	1419
25	S10	-1794	-706	61	DB6	1220	-2369	97	S65	1794	1544
26	S9	-1794	-831	62	DB7	1345	-2369	98	S64	1794	1669
27	S8	-1794	-956	63	TEST	1470	-2369	99	S63	1794	1794
28	S7	-1794	-1081	64		NC		100	S62	1794	1919
29	S6	-1794	-1206	65		NC		101	S61	1794	2044
30	S5	-1794	-1331	66	C1	1794	-2331	102	S60	1794	2169
31	S4	-1794	-1456	67	C2	1794	-2206	103	S59	1563	2369
32	S3	-1794	-1581	68	C3	1794	-2081	104	S58	1438	2369
33	S2	-1794	-1706	69	C4	1794	-1956	105	S57	1313	2369
34	S1	-1794	-1831	70	C5	1794	-1831	106	S56	1188	2369
35	VSS	-1794	-1956	71	C6	1794	-1706	107	S55	1063	2369
36	OSC2	-1794	-2106	72	C7	1794	-1581	108	S54	938	2369
				73				109	S53	813	2369
				74				110	S52	688	23692



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PAD LOCATION(continued)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
109	S53	813	2369	119	S43	-437	2369
110	S52	688	2369	120	S42	-562	2369
111	S51	563	2369	121	S41	-687	2369
112	S50	438	2369	122	S40	-812	2369
113	S49	313	2369	123	S39	-937	2369
114	S48	188	2369	124	S38	-1062	2369
115	S47	63	2369	125	S37	-1187	2369
116	S46	-62	2369	126	S36	-1312	2369
117	S45	-187	2369	127	S35	-1437	2369
118	S44	-312	2369	128	S34	-1562	2369
	S44	-187					

Standard Character Pattern (KS0070B-00)



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