Table 5. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc= 270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire dispaly enable.	37 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	37 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F : 5 X 8 dots/ 5 X 11 dots)	37 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

- "X" : don't care

INTERFACE WITH MPU

1) Interface with 8-bits MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below.

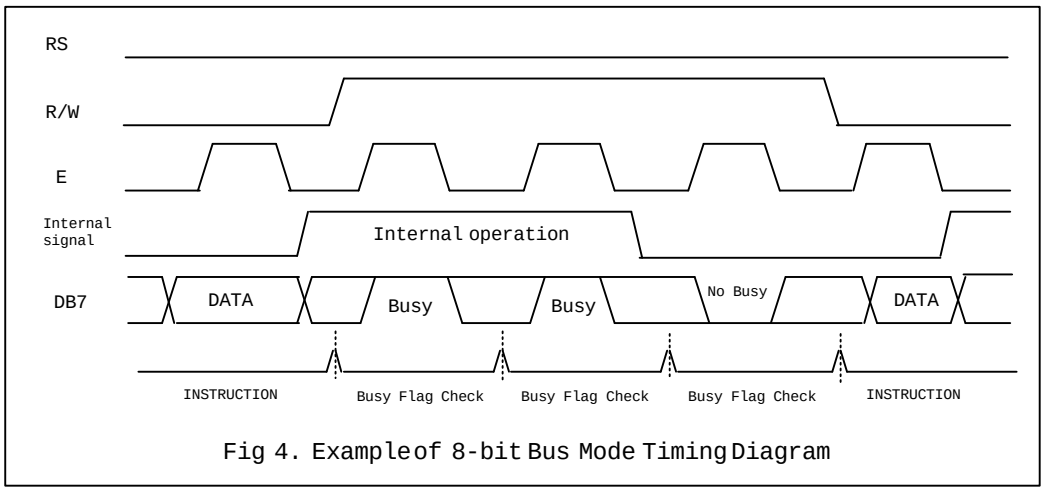

Fig 4. Example of 8-bit Bus Mode Timing Diagram

2) Interface with 4-bits MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended.
Example of timing sequence is shown below.

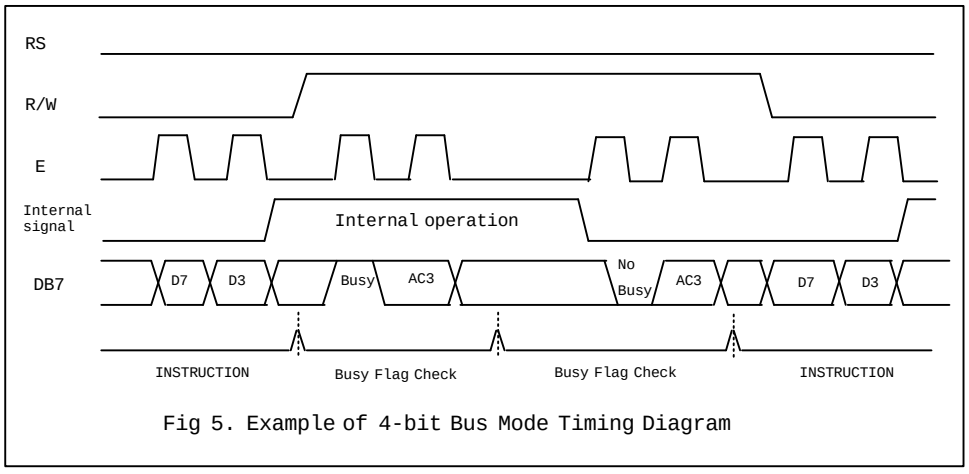

Fig 5. Example of 4-bit Bus Mode Timing Diagram

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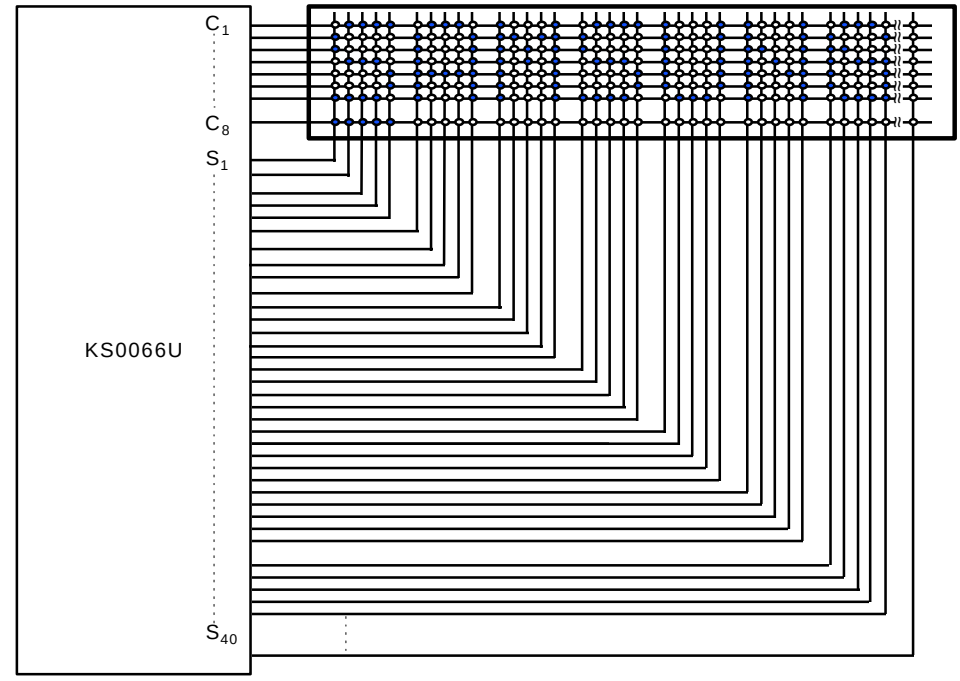
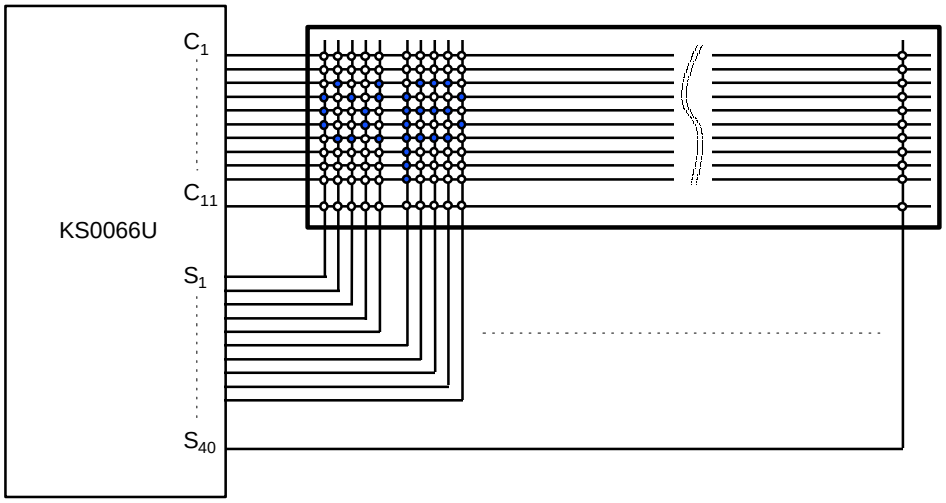
APPLICATION INFORMATION ACCORDING TO LCD PANEL

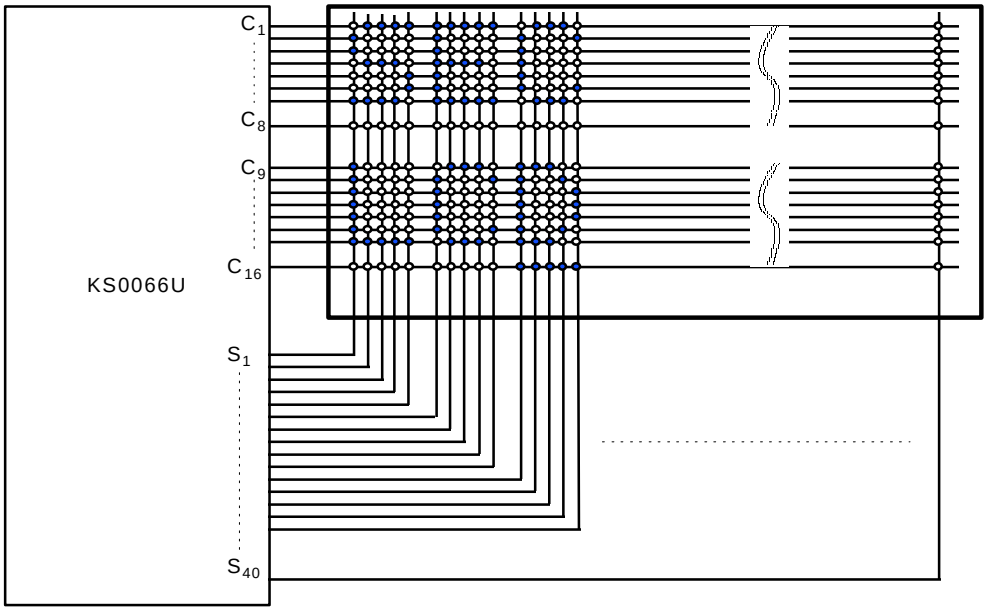
1) LCD Panel: 8 character x 1 line character format; 5 x 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



2) LCD Panel: 8 character x 1 line character format; 5 x 10 dots + 1 cursor line (1/4 bias, 1/11 duty)

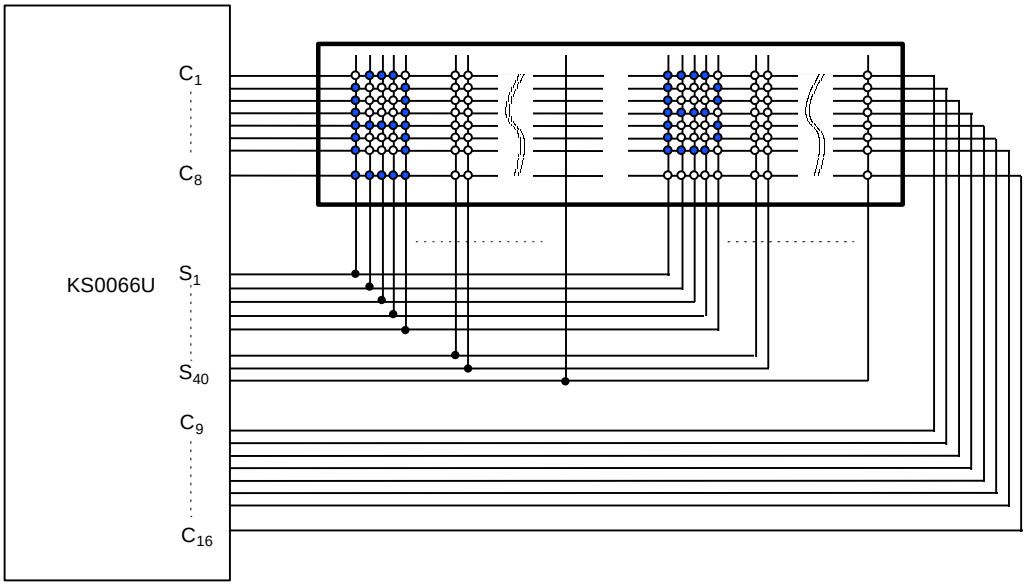


~~3) LCD Panel: 8 character x 2 line character format; 5 x 7 dots + 1 cursor line (1/5 bias, 1/16 duty)~~



4) LCD Panel: 16 character x 1 line

Character format; 5 x 7 dots + 1 cursor line (1/5 bias, 1/16 duty)



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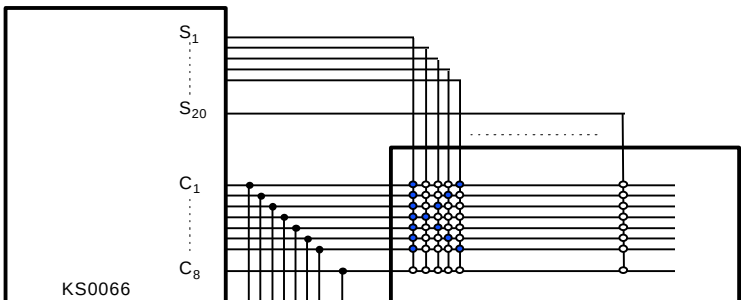
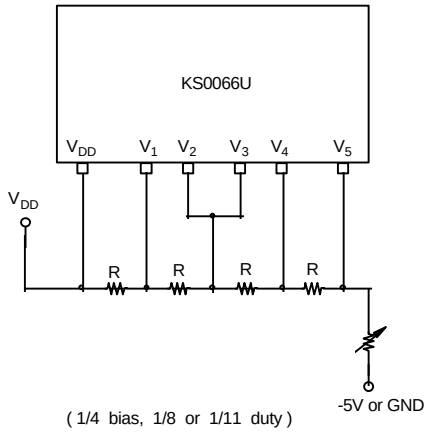
5) LCD Panel: 4 character x 2 line character format: 5 x 7 dots+1 cursor line (1/4 bias, 1/8 duty)

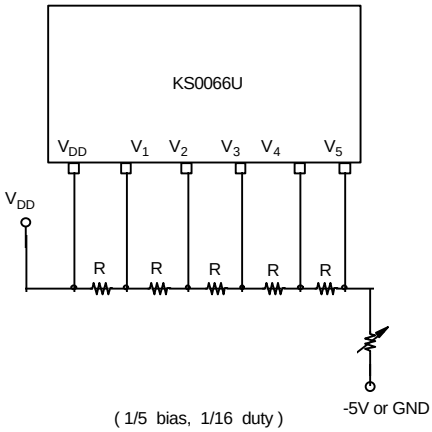


KS0066U

BIAS VOLTAGE DIVIDE CIRCUIT



(1/4 bias, 1/8 or 1/11 duty)



(1/5 bias, 1/16 duty)

INITIALIZING

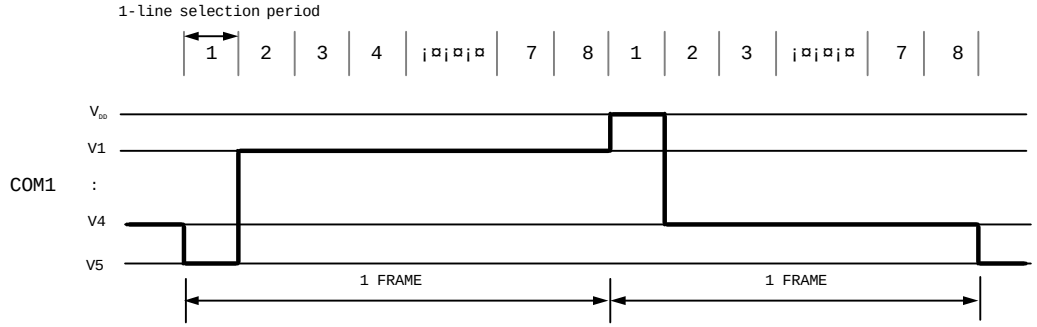
When the power is turned on, KS0066U is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

1) Display Clear instruction
   Write "20H" to all DDRAM
2) Set Function
   DL = 1 : 8 bit interface mode
   N = 0 : 1/8 or 1/11 duty display mode
   F = 0 : 5 X 8 font type
3) Control Display ON/OFF instruction
   D = 0 : Display OFF
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
4) Set Entry Mode instruction
   I/D = 1 : Increment by 1

SH = 0 : No entire display shift

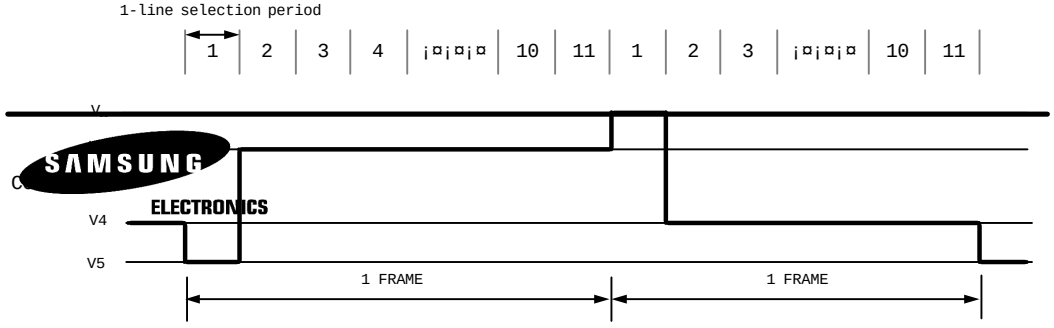
FRAME FREQUENCY

1) 1/8 duty cycle



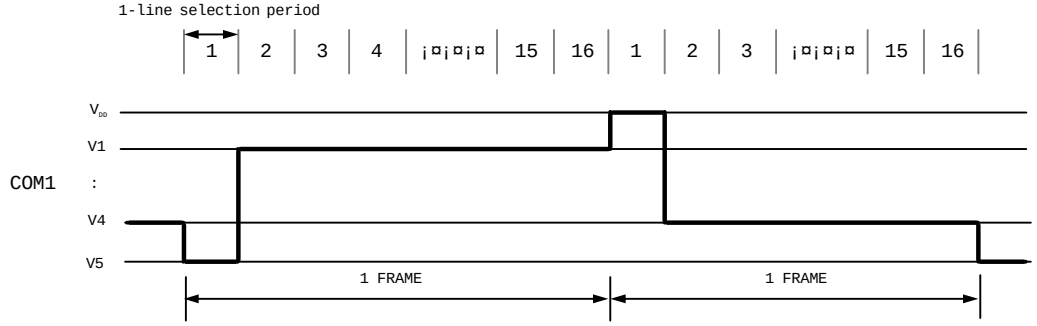
Line selection period = 400 clocks
One Frame = 400 x 8 x 3.7µs = 11850 µs = 11.9 ms (1 clock=3.7 µs,fosc=270kHz)
Frame frequency = 1 / 11.9 ms = 84.3 Hz

2) 1/11 duty cycle



Line selection period = 400 clocks
One Frame = 400 x 11 x 3.7μs = 16300 μs = 16.3 ms (1 clock=3.7 μs,fosc=270kHz)
Frame frequency = 1 / 16.3 ms = 61.4 Hz

3) 1/16 duty cycle



Line selection period = 200 clocks
One Frame = 200 x 16 x 3.7μs = 11850 μs = 11.9 ms (1 clock=3.7 μs,fosc=270kHz)
Frame frequency = 1 / 11.9 ms = 84.3 Hz

INITIALIZING BY INSTRUCTION