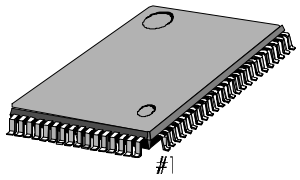
INTRODUCTION

KS0066U is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 1, 2 lines with 5 x 8 or 5 x 11 dots format.

80 QFP-1420C



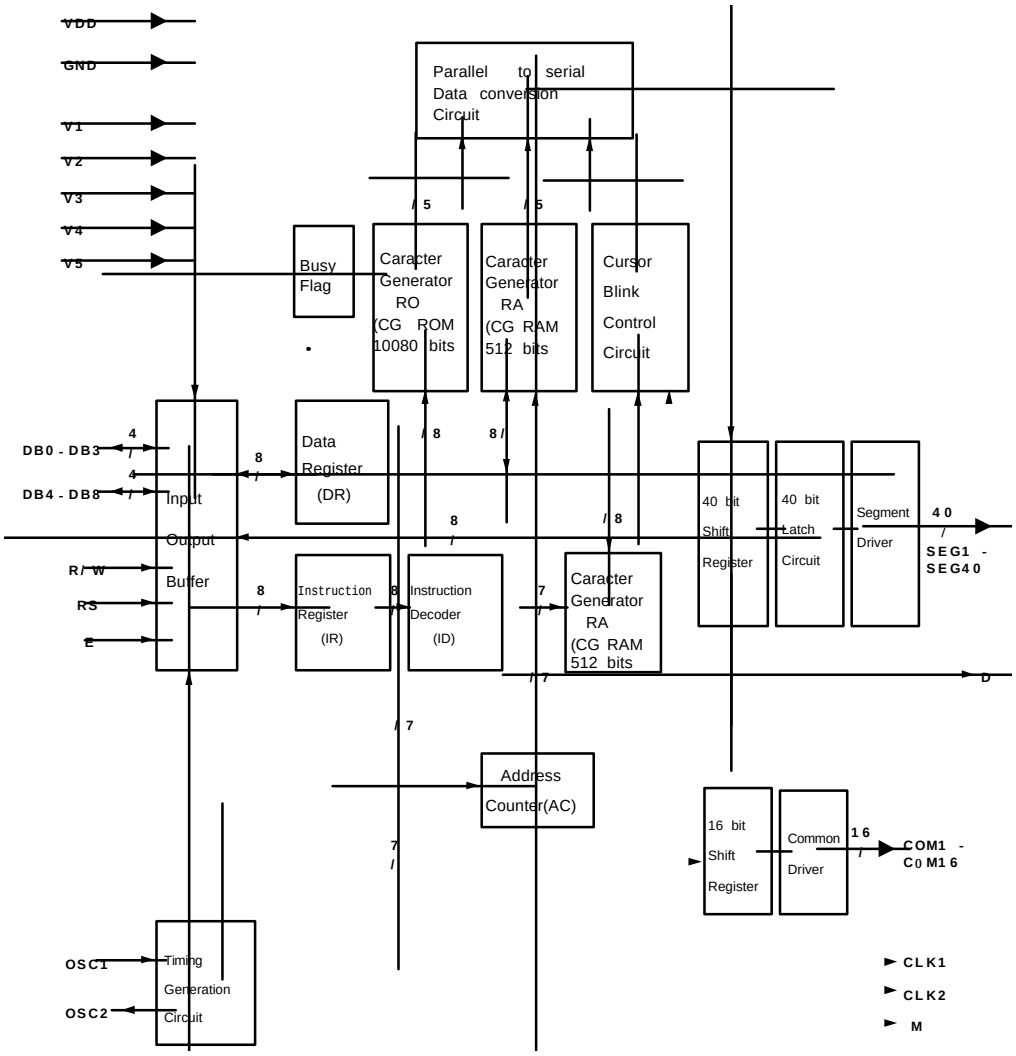
FUNCTIONS

- Character type dot matrix LCD driver & controller.
- Internal driver : 16 common and 40 segment signal output.
- Easy interface with 4-bit or 8-bit MPU.
- Display character pattern : 5 x 8 dots format (204 kinds), 5 x 11 dots format (32 kinds)
- The special character pattern can be programmable by Character Generator RAM directly.
- A customer character pattern can be programmable by mask option.
- It can drive a maximum 80 characters by using the KS0065B or KS0063 externally.
- Various instruction functions.
- Automatic power on reset.

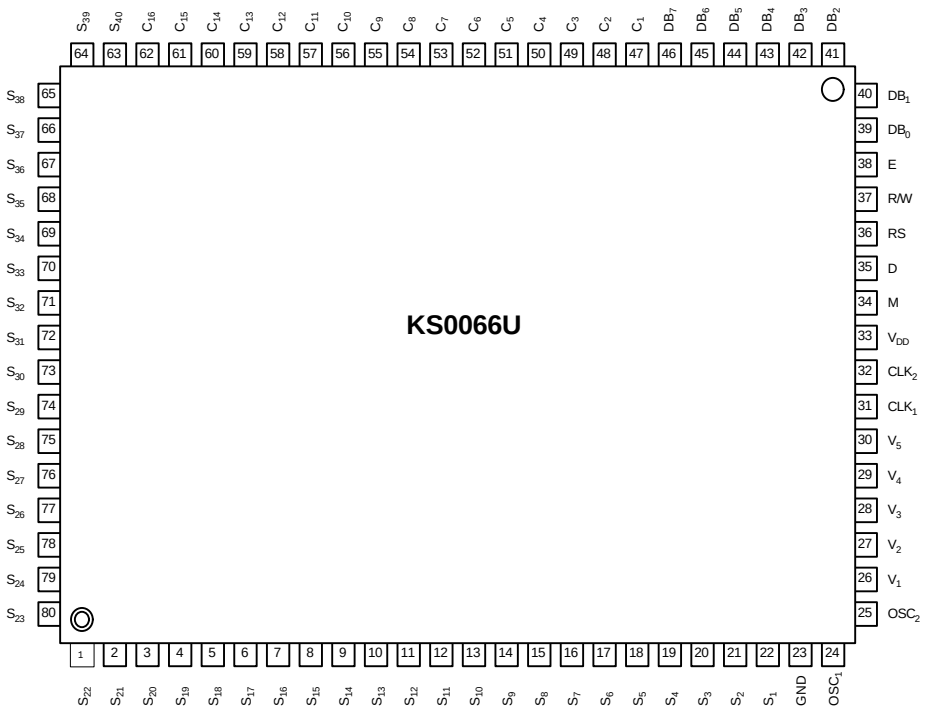
FEATURES

- Internal Memory
  - Character Generator ROM (CGROM) : 10,080 bits (204 characters x 5 x 8 dot) & (32 characters x 5 x 11 dot)
  - Character Generator RAM (CGRAM) : 64 x 8 bits (8 characters x 5 x 8 dot)
  - Display Data RAM (DDRAM) : 80 x 8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range : 2.7 ~ 5.5 V (VDD)
  - LCD drive voltage range : 3.0 ~ 13.0 V (VDD - V5)
- CMOS process
- Programmable duty cycle : 1/8, 1/11, 1/16
- Internal oscillator with an external resistor
- Low power consumption
- 80 QFP or bare chip available

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN(No)	INPUT/ OUTPUT	NAME	DESCRIPTION	INTERFACE
VDD (33)	-	Operating Voltage	for logical circuit (+3V+/-10%,+5V+/-10%)	Power Supply
VSS (GND) (23)			0V (GND)	
V1 ~ V5 (26 ~ 30)		Driver Supply Voltage	Bias voltage level for LCD driving.	
S1 ~ S40 (1~22, 63 ~ 80)	Output	Segment output	Segment signal output for LCD drive.	LCD
C1 ~ C16 (47 ~ 62)	Output	Common output	Common signal output for LCD drive.	LCD
OSC1, OSC2 (24, 25)	Input(OSC1), Output(OSC2)	Oscillator	When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External Resistor/ Oscillator (OSC1)
CLK1,CLK2 (31,32)	Output	Extension driver Latch(CLK1)/ Shift (CLK2) clock	Each outputs extension driver latch clock and extension driver shift clock.	Extension driver
M (34)	Output	Alternated signal for LCD driver output	Outputs the alternating signal to convert LCD driver waveform to AC.	Extension driver
D (35)	Output	Display data interface	Outputs extension driver data (the 41th dot's data)	Extension driver
RS (36)	Input	Register select	Used as register selection input. When RS = "High", Data register is selected. When RS = "Low", Instruction register is selected.	MPU
R/W (37)	Input	Read . Write	Used as read/write selection input. When R/W = "High", read operation. When R/W = "Low", write operation.	MPU
E (38)	Input	Read . write enable	Read . write enable signal.	MPU
DB0 ~ DB3 (39 ~ 42)	Input . Output	Data bus 0 ~ 7	When 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode open these pins.	MPU
DB4 ~ DB7 (43 ~ 46)			When 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output.	MPU

FUNCTION DESCRIPTION

System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

Table 1. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port.
Before executing the next instruction, be sure that BF is not High.

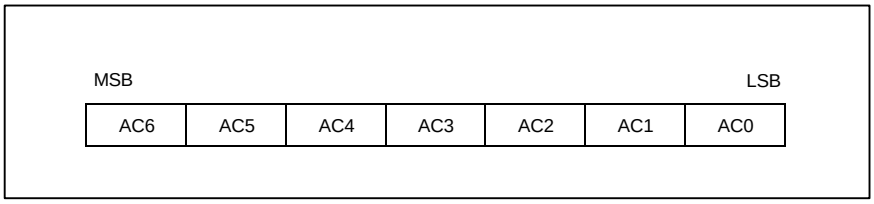
Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Fig-1.)

Fig-1. DDRAM Address



1) 1 line display

In case of 1 line display, the address range of DDRAM is 00H ~ 4FH.
Extension driver will be used. Fig-2 shows the example that 40 segment extension driver is added.

2) 2 line display

In case of 2 line display, the address range of DDRAM is 00H ~ 27H, 40H ~ 67H.
Extension driver will be used. Fig-3 shows the example that 40 segment extension driver is added.

Fig-2. 1-line X 24ch. display with 40 SEG. extension driver.

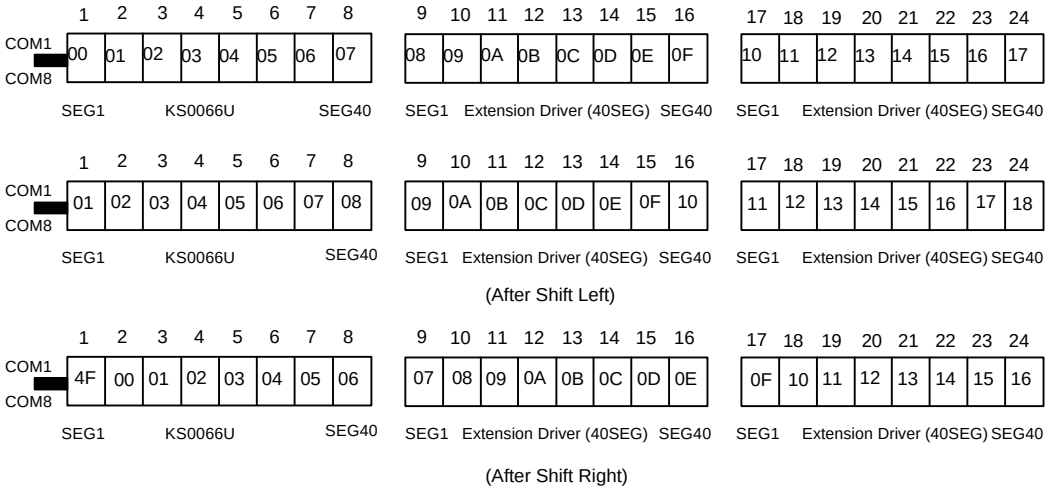
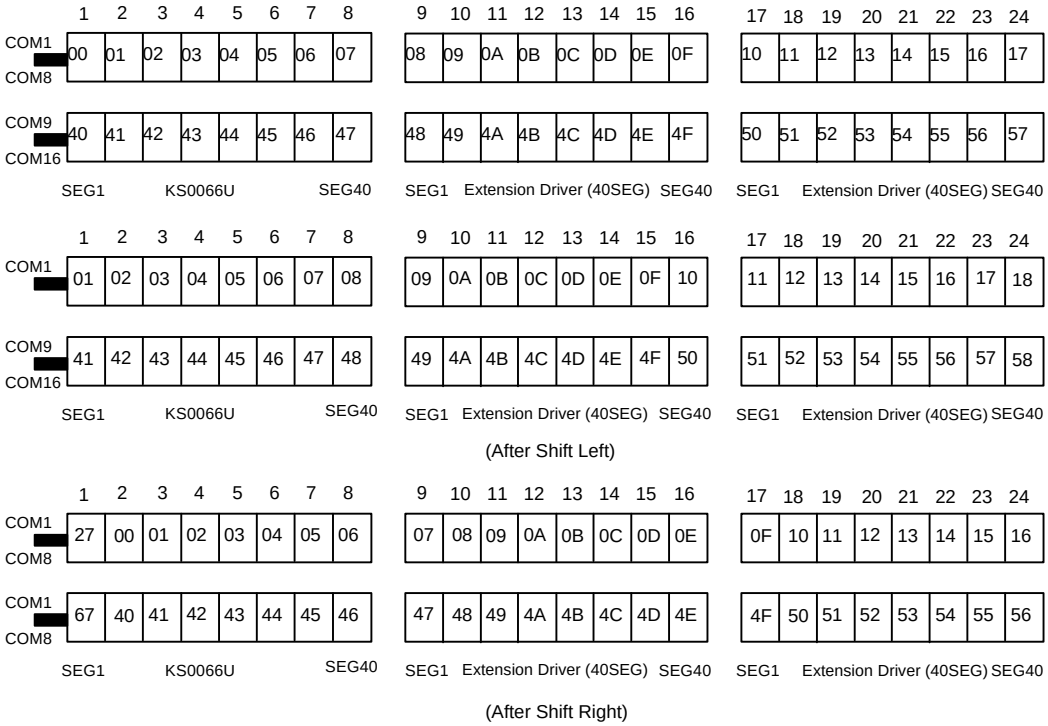


Fig-3. 2-line X 24ch. display with 40 SEG. extension driver.



CGROM (Character Generator ROM)

CGROM has 5 X 8 dot, 208 character, 5 X 11 dot, 32 character pattern. (refer to Table 2)

CGRAM (Character Generator RAM)

CGRAM has up to 5 X 8 dot, 8 characters. By writing font data to CGRAM, user defined character can be used. (refer to Table 3)

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch.
In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11duty , and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

Table 2. Relationship between Character Code(DDRAM) and Character Pattern(CGRAM)

Character Code(DDRAdata)								CGRAaddress			CGRAdata								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	0	①	①	①	0	pattern
											0	0	1				①	0	0	0	①	1
											0	1	0				①	0	0	0	①	
											0	1	1				①	①	①	①	①	
											1	0	0				①	0	0	0	①	
											1	0	1				①	0	0	0	①	
											1	1	0				①	0	0	0	①	
											1	1	1				0	0	0	0	0	
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	①	0	0	0	①	pattern
											0	0	1				①	0	0	0	①	8
											0	1	0				①	0	0	0	①	
											0	1	1				①	①	①	①	①	
											1	0	0				①	0	0	0	①	
											1	0	1				①	0	0	0	①	
											1	1	0				①	0	0	0	①	
											1	1	1				0	0	0	0	0	

"X" : don't care

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of KS0066U and MPU clock, KS0066U performs internal operation by storing control information to IR or DR.
The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5)
Instruction can be divided largely four kinds,

(1) KS0066U function set instructions (set display methods, set data length, etc.)
(2) address set instructions to internal RAM
(3) data transfer instructions with internal RAM
(4) others .

The address of internal RAM is automatically increased or decreased by 1.

* Note : During internal operation, Busy Flag (DB7) is read High.
Busy Flag check must precede the next instruction.

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is incresed by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH = "Low", shift of entire display is not performed.
If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display.
This instruction is used to correct or search display data.(refer to Table 4)
During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
Note that display shift is performed simultaneously in all the line.
When displayed data is shifted repeatedly, each line shifted individually.
When display shift is performed, the contents of address counter are not changed.

Table 4. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display line number control bit
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.

F : Display font type control bit
When F = "Low", it means 5 X 8 dots format display mode
When F = "High", 5 x11 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, accordiing to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.